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# Dual-material Gate Junctionless FET with Vertically Graded Channel Profile for Low Power Applications

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**Abstract**- The metal-oxide-semiconductor field-effect-transistor has dominated the semiconductor industry in the last four decades. To achieve more packaging density with higher speed the technological advancement has been impacted by the performance degradation of these conventional devices due to increased short channel effects namely subthreshold leakage current, subthreshold slope, drain induced barrier lowering etc. With simpler process steps and omission of p-n junctions the junctionless device has been used as an alternative to the ordinary MOSFETs for the low power applications in the nanoscale regime. This paper focus on the dual material gate junctionless FET with vertically graded profile. Comparable value of ON current, reduced OFF current, higher ON-to-OFF current ratio, and lower DIBL with improved subthreshold slope as compared to the conventional double gate junctionless FET with uniform doping profile have been reported.

**Keywords- Dual-material, junctionless FET, graded channel, low power**

## 1. INTRODUCTION

From the late 1960s, the conventional metal-oxide-semiconductor field-effect-transistor (MOSFET) has been used as the prominent building block to realize complementary MOS circuits. The phenomenal progress signified by Moore's law in terms of gaining speed and packaging density has been achieved through the scaling of conventional MOSFETs (Dennard, 1974; Packan, 1999). But, the deviation of electrical performance of conventional MOSFETs in the sub-100 nm region has been attributed to the booming of short channel effects (SCEs) namely threshold voltage roll-off, increased drain induced barrier lowering (DIBL) with degraded subthreshold slope (SS), increased gate leakage current, reliability issues etc (Veeraraghvan et al., 1989; Ghani et al., 2000). To suppress these SCEs in the device structure, the gate controllability over the channel region has been boosted with the development of new multigate architectures (Kranti et al., 2006; Poiroux et al., 2005) like double gate (DG), tri gate, gate-all-around etc. However, due to lower gate capacitance as compared to other multigate devices and flexibility of using in asymmetric mode, the double gate architecture shows its robustness (Poiroux et al., 2005). Nevertheless, while scaling these new architectures, the device engineers faced the challenge of complex realization of ultra steep p-n junctions (Jazeri et al., 2018). Due to uniformly doped silicon film the junctionless field-effect-transistor (JLFET) overcomes this limitation with its structural simplicity (Colinge et al., 2010). With reduced fabrication complexity, the device can be realized with existing CMOS process flow. The device shows bulk conduction which suppresses the mobility degradation with increased temperature due to relaxation of surface scattering mechanism in flat band condition (Lee et al., 2010). In comparison to the conventional MOSFETs, the junctionless FETs show lower leakage current due to absence of reverse biased p-n junctions. This greatly enhances the device suitability for low power applications like dynamic random access memory (DRAM) and biosensor networks (Sahay et al., 2019). But, with the

technological advancement of junctionless device in sub-20 nm regime, drastic increase in DIBL and SS becomes critical. In junctionless FETs the major current component flows through the central part of the channel, hence reducing the doping concentration in the upper and lower part of silicon film may results into significant lowering of the OFF current. Thus, we propose a new dual-gate material DG junctionless FET structure with vertically graded profile (VGP) across the channel. With reduced doping in the upper and lower part of the silicon film and bulk conduction mechanism, the proposed device shows lower OFF state current, reduced DIBL with higher current ratio in sub 20 nm region as compared to the conventional junctionless FETs.

## 2. DEVICE STRUCTURE AND SIMULATION SET-UP

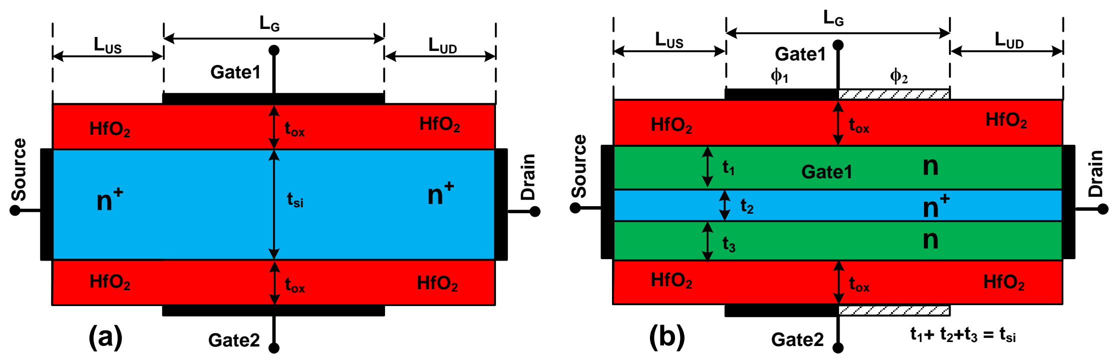


Fig. 1 Schematic diagram of (a) Conventional double gate junctionless FET with uniform doping profile (UDP) (b) Proposed dual-gate material double gate junctionless FET with vertically graded profile (VGP).

The schematic view of uniformly doped conventional DG junctionless FET and the proposed dual-gate material DG junctionless FET with vertically graded profile is shown in Fig. 1. The parameters used in the device simulation have been listed in table 1. Both architectures have been simulated using SILVACO TCAD tool with gate length ($L_G$) of 20 nm and silicon film thickness ($t_{si}$) of 10 nm. The Hafnium oxide ($HfO_2$) was used as high-k dielectric (k=22) to suppress the gate leakage current with effective oxide thickness (EOT) of 01 nm (Choi et al., 2011). The compatibility issues of high-k material with polysilicon gate electrode namely – pinning of Fermi-level and phonon scattering mechanism due to highly doped channel were avoided with application of metal as gate electrode material (Dadgour et al., 2010; Takeuchi et al., 2004). In proposed device, two gate materials with work function $\phi_1$ and $\phi_2$ of value 5.36 eV and 4.86 eV respectively with a difference of 0.5 eV were used to achieve better carrier transport. In case of the proposed device the length ratio $0.5L_G$ for the two different gate materials have been kept constant (Lou et al., 2012). As shown in Fig. 1 (b), the total silicon film has been divided into three parts of thickness of $t_1$, $t_2$ and $t_3$ with $t_1 + t_2 + t_3 = t_{si}$. The values of t1 and t3 have been considered as 04 nm while for $t_2$ 02 nm thickness has been used. Fixed doping concentration of $1\times10^{18}$ cm$^{-3}$ was used in silicon film area with thickness $t_1$ and $t_3$. Whereas, for silicon film area with thickness $t_2$ a higher doping of value $1\times10^{19}$ cm$^{-3}$ has been used. A uniform doping concentration of $1\times10^{19}$ cm$^{-3}$ was taken in conventional DG junctionless device. The impact of high doping and band gap narrowing were considered with *fermi* and *bgn* models respectively. The Shockley-Read-Hall recombination has been modelled with *srh* and the mobility dependence on transverse and longitudinal electric field has been considered using *cvt* model in the simulation (TCAD ATLAS User Manual,

2016). An underlap area with constant length of 10 nm has been used on both source side ($L_{US}$) and drain side ($L_{UD}$) in the two device structures.

Table I. Device simulation parameters used in the SILVACO TCAD tool

| Parameter | Conventional DG JLFET with UDP | DMG DG JLFET with VGP |
|---|---|---|
| Gate length, $L_G$ | 20 nm | 20 nm |
| Silicon film doping concentration, $N_D$ | $1\times10^{19}$ cm$^{-3}$ | $1\times10^{18}$ cm$^{-3}$, $1\times10^{19}$ cm$^{-3}$ |
| Total silicon film thickness, $t_{si}$ | 10 nm | 10 nm |
| Silicon film thickness, $t_1$ | --- | 04 nm |
| Silicon film thickness, $t_2$ | --- | 02 nm |
| Silicon film thickness, $t_3$ | --- | 04 nm |
| Gate electrode work function, $\phi_1$and $\phi_2$ | 5.36 eV | 5.36 eV, 4.86 eV |
| Effective oxide thickness, $t_{ox}$ | 01 nm | 01 nm |
| Length of underlap region towards source end, ($L_{US}$) | 10 nm | 10 nm |
| Length of underlap region towards drain end, ($L_{UD}$) | 10 nm | 10 m |

## 3. RESULTS AND DISCUSSION

Based on the device simulation set-up and parametric values listed in table1 following results for the two structures have been observed. In this section the curves represented by solid symbols depicts the results of DMG JLFET with vertically graded channel profile while the curves with open symbol are related to SMG JLFET with uniform doping profile.

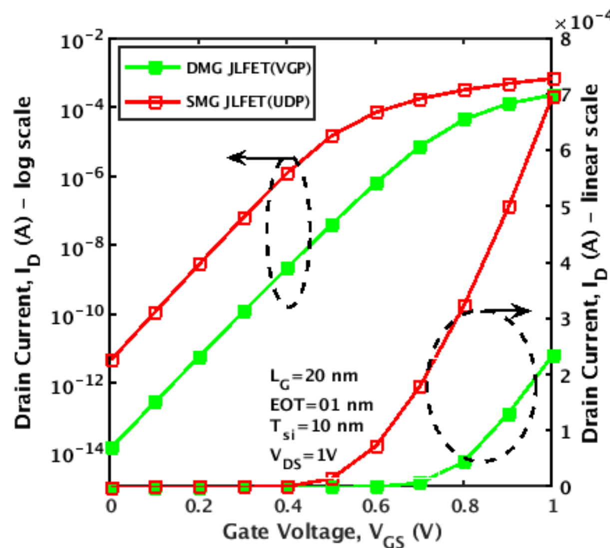


Fig. 2 Comparison of drain current ($I_D$) vs. gate voltage ($V_{GS}$) characteristics for single material gate junctionless FET with uniform doping profile and dual material gate junctionless FET with vertically graded profile.

The drain current ($I_D$) for conventional and proposed junctionless FET has been compared on linear and logarithmic scale in fig. 2. The curve shown in the fig. 2 has been obtained in saturation region for drain-source voltage of 1.0V. Due to the application of dual material on the gate electrode the value of vertical electric field on the drain end is lowered and the proposed devices shows comparable ON current ($I_{ON}$) in the range of $10^{-4}$ (A/µm).

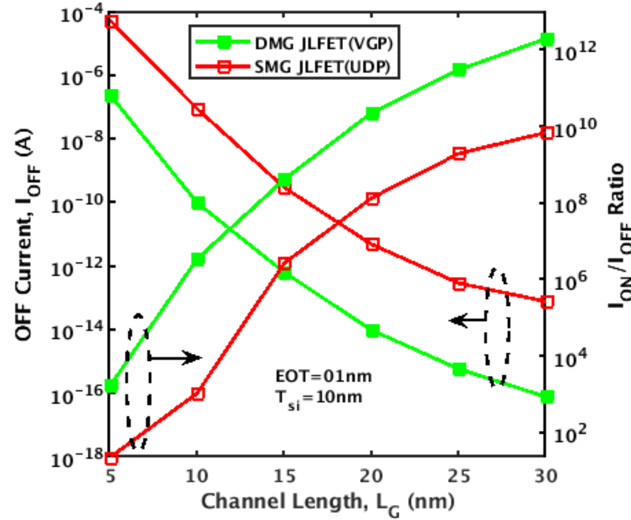


Fig. 3 Comparison of OFF current ($I_{OFF}$) and current ratio ($I_{ON}/I_{OFF}$) for single material gate junctionless FET with uniform doping profile and dual material gate junctionless FET with vertically graded profile.

The impact of gate length scaling on various performance parameters of both device have been presented in fig. 3. Here, it can be observed that comparatively lower $I_{OFF}$ have been shown by the DMG JLFET with graded doping profile within the range of gate length from 30 nm to 5 nm. This has been attributed to the reduced value of doping concentration near the oxide-semiconductor interface which leads to lesser number of charge carriers in the device. Here, it can be observed, that at lower technology nodes the conventional junctionless FETshows the $I_{OFF}$ of the order of $10^{-4}$ (A/µm), which detreorates the $I_{ON}/I_{OFF}$ ratio below $10^2$. However, the proposed junctionless device shows the current ratio of the order of $10^3$ even for the gate length of 5 nm due to lower OFF current as shown in fig. 3.

As the gate length shrinks the interaction between drain and source region increases. This is due to impact of increased drain voltage which leads to barrier lowering at source-channel interface. The barrier lowering at source end eases the introduction of charge carrier from source into the channel and reduction in threshold voltage of the device. Hence, more DIBL value has been observed with gate length scaling. However, due to vertically graded channel, lower number of charge carriers are introduced in the proposed junctionless device, hence lesser value of DIBL has been observed as compared to the conventional junctionless FET as shown in fig. 4. From fig. 4 it can also be noted that the proposed device shows comparable subthreshold slope as compared to the conventional junctionless device, but improves at lower technology node below 10 nm. Qualitatively, the reduction in doping concentration results in to trivial lowering of ON current, but significant reduction in OFF current, which leads to lowering of subthreshold slope for the proposed device.

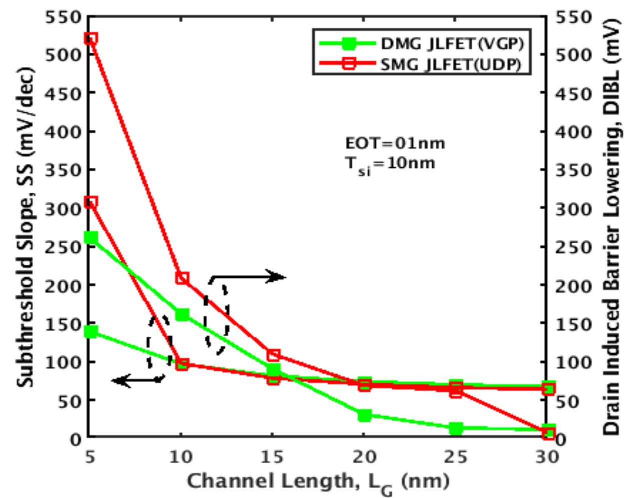


Fig. 4 Comparison of drain induced barrier lowering and subthreshold slope for single material gate junctionless FET with uniform doping profile and dual material gate junctionless FET with vertically graded profile.

## 4. CONCLUSIONS

The electrical performance of proposed dual material gate junctionless FET with vertically graded profile has been compared with the conventional junctionless FET. Due to vertically graded channel, lower numbers of charge carriers are allowed in the silicon film. As a result, the proposed device shows improved characteristics in terms of lower $I_{OFF}$, reduced DIBL, higher $I_{ON}/I_{OFF}$ ratio and improved SS with scaling of physical gate length. It is also concluded that with lower $I_{OFF}$ and comparable $I_{ON}$ the proposed device can be a used as a potential candidate to realize the circuits in low power applications.

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